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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,804	12/28/2001	Takashi Miura	217806US2	3091

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EXAMINER	
BONZO, BRYCE P	

ART UNIT	PAPER NUMBER
2114	7

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,804	MIURA ET AL.	
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,13,15-18,20 and 21* is/are rejected.

7)☒ Claim(s) *6-12,14,19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claim 4 is rejected under 35 USC §112.

Claims 1-3,13, 15-17 and 20 are rejected under 35 USC §102.

Claims 5, 18 and 21 are rejected under 35 USC §103.

Claims 6-12, 14, 19 and 22 are objected while containing allowable matter.

Rejections under 35 USC §112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 4 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites "the memory access" in line four. The is not proper antecedent basis for this limitation. Additionally, the claim describes sending a memory access to a main bus (specifically "for said main bus"). Main buses are not conventionally the target of a memory access (as the main bus has no storage). The Examiner believes in light of the specification and a general knowledge of computer architecture the Applicant has mistranslated the concept of the debugging module issuing a DMA transfer (direct memory access) received from the debugging tool and placing the transfer on internal main bus. As the Examiner is uncertain whether the claim as written (assuming "the

memory access" is corrected to read "a memory access") or the above interpretation is correct, the Examiner has not examined the claim on the merits against the prior art. Applicant is advised that should the only amendment to the claim be a correction of antecedent basis, that a rejection under 35 USC §112, first paragraph is likely as the claim would recite an unsupported and unconventional bus and memory schema.

Rejections under 35 USC §102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 and 13, 15-17 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Dervisoglu (United States Patent No 6,687,865 B1).

As per claim 1, Dervisoglu discloses:

A semiconductor integrated circuit comprising:

an internal main bus (Figure 1b, item 105);

first and second microprocessors (Figure 1b, items 106) sharing said internal main bus (figure 1b, item 105);

a first debug serial bus with one end thereof connected to said first microprocessor (Figure 1b, item 102 wrapped around the 3rd party core);

a second debug serial bus with one end thereof connected to said second microprocessor (Figure 1b, item 102, wrapped around the user developed core); and

a debugging module connected to the other ends of said first and second debug serial buses (Figure 1b, item 101) and transferring at least a debugging program and debugging data to said first microprocessor via said first debug serial bus and to said second microprocessor via said second debug serial bus (column 14, lines 26-31 describe downloading programming; column 4, lines 43-48 describe downloading bitmaps data for use by the processors under test).

As per claim 2, Dervisoglu discloses:

a dedicated external debugging terminal which connects said debugging module and a debugging tool for controlling a debugging task in accordance with a debugging program (column 14, lines 43-54).

As per claim 3, Dervisoglu discloses:

wherein said debugging module is directly connected to said internal main bus (figure 1b, main bus 101 is connected to debugging module 105).

As per claim 13, Dervisoglu discloses:

said first microprocessor comprises a first bus interface unit connected not only to a microprocessor core thereof but also to said first debug serial bus and said internal main bus; and said second microprocessor comprises a second bus interface unit connected not only to a microprocessor core thereof but also to said second debug serial bus and said internal main bus. Dervisoglu discloses the cores as being connected to the bus interface block, and shows the serial debug buses (which contain scan chaining registers) specifically crossing through this boundary. Boundary scan chains always monitor the interface to the main bus of a device being monitored. It is required, as a boundary scan test monitors all input and output of the device. Thus the interface to the main bus and the debug buses must be incorporated into a respective interfaces for each core under test.

As per claim 15, Dervisoglu discloses:

a wiring board (column 14, lines 37-47; a board tester tests devices on a board);

a semiconductor integrated circuit which comprises an internal main bus (figure 1b, item 105), first and second microprocessors (Figure 1b, items 106) sharing said internal main bus figure 1b, item 105), a first debug serial bus with one end thereof connected to said first microprocessor (Figure 1b, item 102 wrapped around the 3rd party core), a second debug serial bus with one end thereof connected to said second microprocessor (Figure 1b, item 102, wrapped around the user developed core), and a debugging module connected to the other ends of said first and second debug serial buses (Figure 1b, item 101) and transferring at least a debugging program and

debugging data to said first microprocessor via said first debug serial bus, and to said second microprocessor via said second debug serial bus(column 14, lines 26-31 describe downloading programming; column 4, lines 43-48 describe downloading bitmaps data for use by the processors under test); and

a memory mounted on said wiring board and storing at least debugging data (column 6, lines 21-37).

As per claim 16, Dervisoglu discloses:

further comprising an input/output interface circuit mounted on said wiring board (figure 1b shows a bridge to a peripheral bus which constitutes an I/O controller).

As per claim 17, Dervisoglu discloses:

comprising a dedicated debug interface terminal which connects said debugging module of said semiconductor integrated circuit and a debugging tool for controlling a debugging operation in accordance with a debugging program (column 12, lines 11-30).

As per claim 20, Dervisoglu discloes:

a wiring board (column 14, lines 37-47; a board tester tests devices on a board);

a semiconductor integrated circuit which comprises an internal main bus (figure 1b, item 105), first and second microprocessors (Figure 1b, items 106) sharing said internal main bus figure 1b, item 105), a first debug serial bus with one end thereof connected to said first microprocessor (Figure 1b, item 102 wrapped around the 3rd

party core), a second debug serial bus with one end thereof connected to said second microprocessor (Figure 1b, item 102, wrapped around the user developed core), and a debugging module connected to the other ends of said first and second debug serial buses (Figure 1b, item 101) and transferring at least a debugging program and debugging data to said first microprocessor via said first debug serial bus, and to said second microprocessor via said second debug serial bus(column 14, lines 26-31 describe downloading programming; column 4, lines 43-48 describe downloading bitmaps data for use by the processors under test); and

a memory mounted on said wiring board and storing at least debugging data (column 6, lines 21-37) and

a debugging tool connected to said debugging module of said semiconductor integrated circuit (column 14, lines 43-54).

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 18 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dervisoglu (United States Patent No 6,687,865 B1).

As per claim 5, Dervisoglu discloses:

an input / output controller connected to said internal main bus (figure 1b shows a bridge to a peripheral bus which constitutes an I/O controller).

Dervisoglu does not explicitly disclose:

memory controller *and* a direct memory access controller all of which are connected to said internal main bus. The Examiner takes Official Notice that the placement of a memory controller and a DMA controller on an internal bus is a notoriously well known in the computer arts. Placing memory and DMA controllers in computer has long been used to enhance the speed of computer systems by removing menial work from the processor, specifically data transfers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory and DMA controllers into the system of Dervisoglu in order to optimize the computer for modern computing practices.

As per claim 18, Dervisoglu discloses:

an input / output controller connected to said internal main bus (figure 1b shows a bridge to a peripheral bus which constitutes an I/O controller).

Dervisoglu does not explicitly disclose:

memory controller *and* a direct memory access controller all of which are connected to said internal main bus. The Examiner takes Official Notice that the placement of a memory controller and a DMA controller on an internal bus is a notoriously well known in the computer arts. Placing memory and DMA controllers in

computer has long been used to enhance the speed of computer systems by removing menial work from the processor, specifically data transfers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory and DMA controllers into the system of Dervisoglu in order to optimize the computer for modern computing practices.

As per claim 21, Dervisoglu discloses:

an input / output controller connected to said internal main bus (figure 1b shows a bridge to a peripheral bus which constitutes an I/O controller).

Dervisoglu does not explicitly disclose:

memory controller *and* a direct memory access controller all of which are connected to said internal main bus. The Examiner takes Official Notice that the placement of a memory controller and a DMA controller on an internal bus is a notoriously well known in the computer arts. Placing memory and DMA controllers in computer has long been used to enhance the speed of computer systems by removing menial work from the processor, specifically data transfers. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory and DMA controllers into the system of Dervisoglu in order to optimize the computer for modern computing practices.

Allowable Subject Matter

Claims 6-12, 14, 19 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter. The italicized portions below in combination with the remaining limitations overcome the prior art.

As per claims 6, 7, 19 and 22:

a first debug supporting unit provided in said first microprocessor and controlling a debugging function of said first microprocessor; and

a second debug supporting unit provided in said second microprocessor and controlling a debugging function of said second microprocessor;

a first debug controlling bus which connects said first debug supporting unit and said debugging module; and

a second debug controlling bus which connects said second debug supporting unit and said debugging module.

As per claim 12:

wherein said *debugging module optionally demands each of said first and second microprocessors to delay returning to a user mode from a debugging mode.*

As per claim 14:

wherein: said first bus interface unit comprises an internal main bus/debug serial bus controlling circuit connected to said debugging module and said microprocessor core, a parallel-to-serial converting circuit connected to said debugging module and said internal main bus/debug serial bus controlling circuit, a serial-to-parallel converting circuit connected to said debugging module and said parallel-to-serial converting circuit, and a selector connected to said microprocessor core, said internal main bus/debug serial bus controlling circuit, said parallel-to-serial converting circuit and said serial-to-parallel converting circuit; and said second bus interface unit comprises an internal main bus I/O debug serial bus controlling circuit connected to said debugging module and said microprocessor core, a parallel-to-serial converting circuit connected to said debugging module and said main bus/debug serial bus controlling circuit, a serial-to-parallel converting circuit connected to said debugging module and said parallel-to-serial converting circuit, and a selector connected to said microprocessor core, said internal main bus/debug serial bas controlling circuit, said parallel-to-serial converting circuit and said serial-to-parallel converting circuit.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834 or upon moving to the new facilities in Alexandria (571) 272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713 or upon moving to the new facilities in Alexandria (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo
Examiner
Art Unit 2114

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